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Improved interface state density by low temperature epitaxy grown AlN for AlGaN/GaN metal-insulator-semiconductor diodes

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ABSTRACT

AlGaN/GaN metal-insulator-semiconductor (MIS) diodes were fabricated using low temperature epitaxy (LTE) grown AlN at 200 °C, a technique combining both physical vapor deposition and chemical vapor deposition. The interface trap characteristics of the MIS-diodes were investigated using the frequency dependent parallel conductance method. Two distinct interface trapping regions were observed, where the fast interface traps had an estimated density (D_{it}) as low as 6.7×10^{11} cm^{-2} eV^{-1} while the slow interface traps D_{it} were as low as 6.8×10^{11} cm^{-2} eV^{-1}. About 3.8 × improvement in D_{it} was achieved compared to our previous work by optimization of the LTE deposition conditions. The fast traps are located within the energy interval of 0.24–0.30 eV below the conduction band while the slow traps are located 0.44–0.56 eV below the conduction band. The observed fast traps were associated with the AlGaN/GaN interface, while the observed slow traps may have formed at AlN/GaN interface during the deposition of AlN by LTE.

1. Introduction

GaN based high-electron-mobility transistors (HEMTs) are excellent for high-frequency high-power applications. However, there are still problems faced by these devices such as current collapse and self-heating [1–5]. Si_3N_4 is the most widely used passivation layer for suppressing the current collapse. However, its poor thermal conductivity (10 WK^{-1} m^{-1}) prevents suppression of self-heating of the device. As an alternative, researchers have explored the use of high thermal conductivity AlN (285 WK^{-1} m^{-1}) as a passivation layer to reduce self-heating and to suppress the current collapse [6]. Tanaka et al [7] has previously employed a thick AlN layer to suppress self-heating from AlGaN/GaN HEMTs. It was shown that thicker layers (0.5–1 μm) of AlN allowed for increased suppression of self-heating. Passivation with wide bandgap AlN (6.0 eV) has an added advantage of improving device breakdown voltage in comparison to conventional SiN passivation in AlGaN/GaN HEMTs [1].

It is essential to have thick AlN in AlGaN/GaN HEMTs as a passivation layer to suppress the self-heating from the fabricated devices [7]. One possible way for AlN deposition is by metal–organic chemical vapor deposition (MOCVD) [8]. However, the growth temperature of AlN is > 600 °C, which is not desirable for the fabrication of AlGaN/GaN HEMTs. A lower growth temperature also has the advantage of improving device performance and preventing tensile strain-induced cracking of AlN layer in AlN based MIS-HEMTs [9,10]. Though plasma-enhanced atomic layer deposition (PEALD) based AlN films exhibit excellent interface state density (D_{it}) on GaN at low temperatures [11,12], the realization of thick (0.5–1 μm) AlN deposition by PEALD is not possible due to its very low deposition rate. Recently, Dikme et al. [13] have successfully grown single crystalline AlN layers on Si and sapphire substrates with thicknesses up to 1 μm even at 200 °C, using a novel technique called low temperature epitaxy (LTE). This technique enables the deposition of thick AlN films as it is a combination of physical vapor deposition (PVD) and chemical vapor deposition (CVD). However, before LTE-AlN can be used as a passivation layer to reduce self-heating, the LTE-AlN/GaN interface must be quantified. For switching applications, it is important to investigate the interface traps as they could degrade device switching properties through the charging and discharging phenomenon [14]. To investigate the interface traps, LTE-AlN MIS-diodes with a thickness of ~ 8.5 nm were fabricated and measured using conductance method. For a fair comparison with prior art by MOCVD and PEALD, we have also selected ~ 8 nm thick AlN as a dielectric layer for this study. Previously, the authors have reported the interface trap properties using the LTE grown AlN [15]. However, the interface trap density is about 2.6×10^{12} cm^{-2} eV^{-1}. Hence, further improvement of the interface trap properties is essential to have

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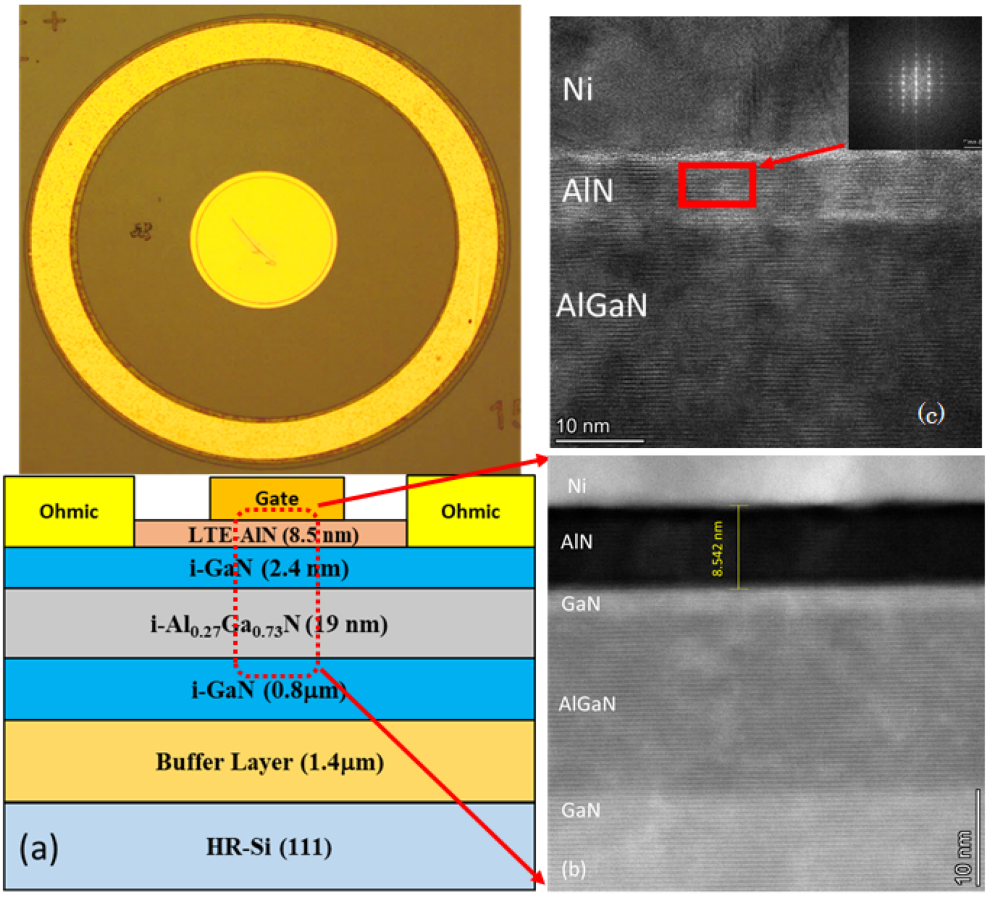

Fig. 1. (a) Optical image of AlN MIS-diode with its corresponding schematic cross-section, where the dotted line indicated the TEM location, (b) cross-sectional STEM image of the Gate region, and (c) Cross-sectional HRTEM image of the Ni/AlN/GaN interface. Inset: digital diffraction pattern of AlN layer obtained by FFT.

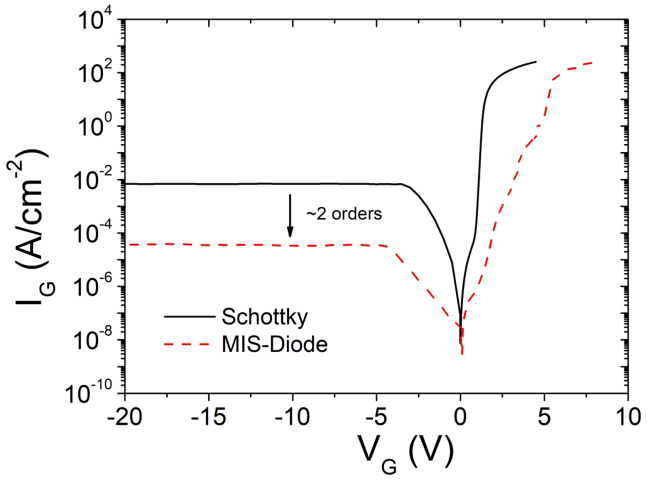

Fig. 2. Diode I-V Curves compared Schottky and MIS-diodes of the same size (100 µm diameter circle diodes).

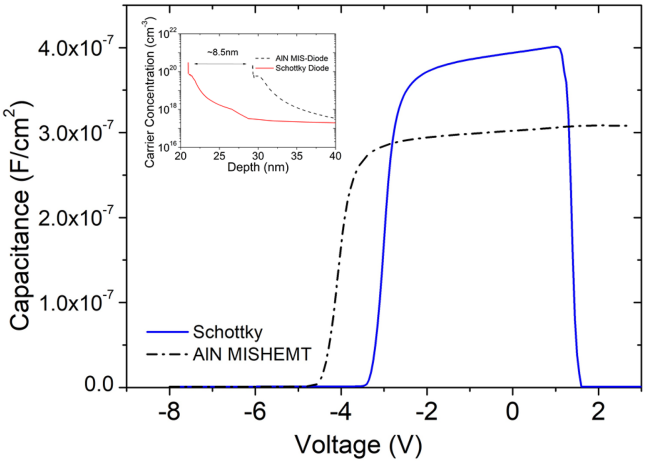

Fig. 3. C-V characteristics and depth-carrier concentration profile (insert) of LTE-AlN AlGaN/GaN MIS-diode and conventional diode at 1 MHz.

improved device characteristics. In this study, we report the improvement of the LTE grown AlN which exhibits lower interface trap density than that reported previously. The main improvement compared to previous reports of LTE-AlN comes from the more precise optimization of the deposition conditions [15]. In this work, in order to reduce interface state density, we have prevented the surface damages during the deposition of AlN on GaN by (i) surface cleaning with very low energy H_2 plasma (10% of the plasma compared with the AlN deposition), (ii) thin seeding layer deposition with 50% of the plasma power and (iii) annealing of the seeding layer by nitrogen plasma. This condition was maintained for the deposition of ~ 8 nm thick AlN on GaN. Detailed analysis was also carried out to investigate the traps characteristics (fast and slow traps).

2. Experimental

The AlGaN/GaN HEMT structure on Si substrate was grown by MOCVD technique. It exhibited room temperature sheet resistance of 591 Ω/□, a Hall mobility of 1440 $cm^2V^{-1}s^{-1}$ and a sheet concentration

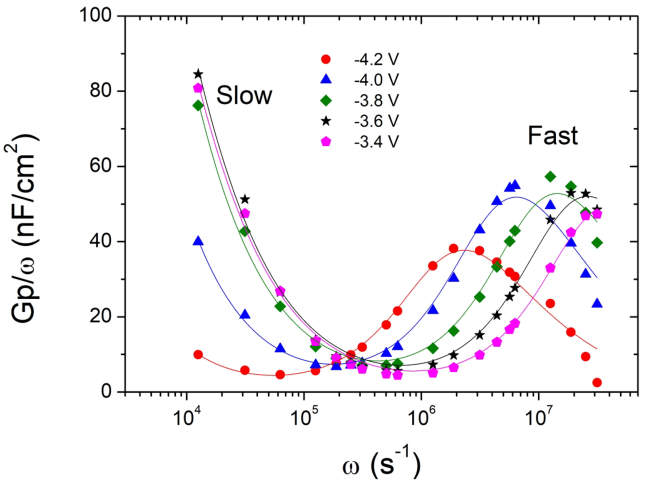

Fig. 4. Gp/ω versus radial frequency plot for different gate voltages of LTE-AlN MIS-diode (solid lines are fitting curves).

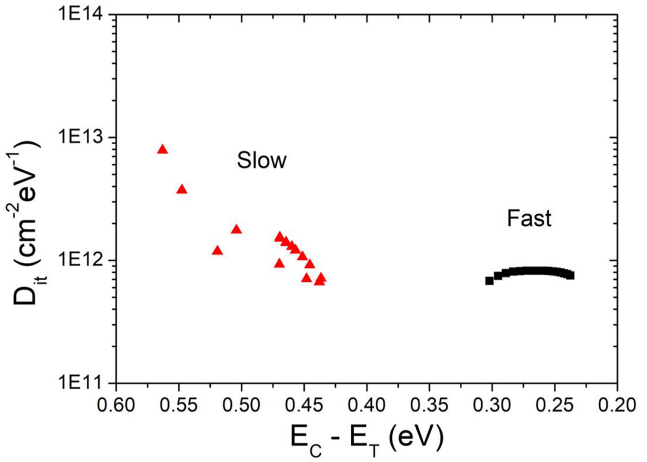

Fig. 5. Distribution of interface state density and trap state time constant as a function of the gate voltage of LTE-AlN MIS-diode.

Table 1
Benchmarking of extracted D_{it} values from AlN/GaN MIS diodes with other deposition technique.

Deposition Method	Thickness (nm)	Dep Temp (°C)	D_{it} (cm^{-2} eV^{-1})
PEALD	3	300	3×10^{12} [11]
PEALD	20	300	3.1×10^{11} [12]
In-situ MOCVD	11	1120	4.5×10^{12} [25]
In-situ MOCVD	5	600	1.1×10^{11} [8]
LTE	6	200	2.6×10^{12} [15]
LTE (This work)	**8.5**	**200**	**6.8×10^{11}**

of 7.35×10^{12} cm^{-2} [16]. The device fabrication process started with mesa isolation by reactive ion etching (RIE) using a Cl_2/BCl_3 mixture. The ohmic contacts consisting of Ti/Al/Ni/Au (20/120/40/50 nm) were deposited followed by rapid thermal annealing at 825 °C for 30 s in an N_2 atmosphere. Transmission line measurements showed a contact resistance of 0.4 Ωmm.

The single crystalline AlN was grown by low temperature epitaxy (LTE) at 200 °C for a thickness of ~ 8 nm. To grow single crystalline AlN, a high surface mobility of the Al- and N- atoms are required. Standard growth methods use a high temperature deposition to achieve this surface mobility. However, in our LTE deposition, the surface mobility of Al- and N- atoms were enhanced by a combination of two different plasma sources. This helped to achieve sufficient surface mobility of Al- and N- atoms for the growth of single crystalline AlN at around 200 °C. First, the sample was cleaned with a weak Ar/H_2 plasma to remove the native oxide. Next, an initial AlN layer was grown using nitrogen rich conditions. The AlN seeding layer (~0.5 nm) was grown at a sufficiently low plasma power to prevent damage of the GaN surface. This thin layer was then annealed in a nitrogen plasma to improve the AlN seed layer quality and to ensure that it continues the GaN lattice structure. The remaining AlN was then grown at a higher plasma power to the desired thickness of ~ 8 nm. Further LTE-AlN deposition details, including those used in previous reports [15], and typical LTE-AlN characterization can be found in Dikme et al [13]. After the LTE-AlN deposition, a Ni/Au (50/200 nm) layer was then deposited to form the gate contact. Further metal thickening (10/400 Ti/Au) was also performed after AlN etching, with RIE with a gas mixture of Cl_2/BCl_3/Ar (40/20/10 sccm) at 250 W.

Fig. 1 shows the (a) schematic cross-section of the fabricated AlN/AlGaN/GaN MIS diode and (b) cross-sectional STEM image of Ni/AlN/GaN/AlGaN/GaN interface. Single crystalline nature of the grown AlN has been realized using high resolution transmission electron microscopy (HRTEM) (see Fig. 1(c)). The digital diffraction pattern obtained by fast Fourier transform (FFT) of AlN layer (as seen in the inset of Fig. 1(c)) reveals a high-quality single crystal of hexagonal AlN with [0001] orientation perpendicular to the substrate surface, indicating this technique can produce single crystalline AlN. For comparison, the conventional Ni/Au Schottky devices were also fabricated on the same HEMT structure [16]. The current–voltage (I-V), capacitance–voltage (C-V) and conductance-frequency (C-F) measurements were carried out at room temperature using an Agilent B1505A power device analyzer.

3. Results and discussion

The I-V characteristics of conventional Schottky diode and AlN/GaN/AlGaN/GaN MIS-diode can be seen in Fig. 2. The insertion of 8.5 nm of LTE-AlN causes two orders of magnitude lower gate leakage current at −20 V and five orders of magnitude lower forward current at 2 V, compared to the conventional Schottky diode. A forward gate voltage as high as + 4.6 V can be reached at gate current density of 1 A/cm^2, which is comparable to the AlN/GaN MIS-diodes at + 5.3 V using thermally grown ALD technique [17].

Typical C-V Characteristics of an LTE grown AlN/GaN MIS-diode and a conventional Schottky diode at 1 MHz can be seen in Fig. 3. A zero-bias capacitance of 373 nF/cm^2 and 302 nF/cm^2 for 200 μm conventional diode and MIS diode were obtained, respectively. Using the C-V curves, a concentration versus depth profile (Fig. 3 inset) was calculated using equation (1),

$$d_{AlN} = \frac{\varepsilon_{AlN}\, d_{2DEG}}{\varepsilon_{AlGaN}} \left(\frac{C_{MIS-Diode}}{C_{Diode}} - 1 \right) \quad (1)$$

where ε_{AlN} and ε_{AlGaN} are the dielectric permittivity of AlN (9.14) and AlGaN layer (9.0), respectively [18,19]. $C_{MIS\text{-}Diode}$ and C_{Diode} are the capacitance of MIS-diode and conventional Schottky diode, respectively. The thickness of the AlN dielectric layer was estimated to be ~ 8 nm, which agrees well with the cross-sectional TEM image showing ~ 8.5 nm (Fig. 1(b)).

Frequency-dependent conductance measurements were performed at selected biases to estimate the D_{it} and trap time constant (τ_{it}) at the AlN/GaN interface [20]. The frequency was varied from 1 kHz to 5 MHz over the gate voltage (V_g) range of −4.2 V to −3.4 V. Fig. 4 shows the parallel conductance (G_p) G_p/ω versus ω for the same V_g range. The two peak regions in the G_p/ω plots correspondingly indicate the presence of both low frequency (slow traps) and high frequency (fast traps). Assuming a continuum of trap energy levels, G_p can be expressed as

$$\frac{G_p}{\omega} = qD_{its}\left(\frac{ln(1+\omega^2\tau_s^2)}{2\omega\tau_s}\right) + qD_{itf}\left(\frac{ln(1+\omega^2\tau_f^2)}{2\omega\tau_f}\right) \quad (2)$$

where ω is the radial frequency, D_{its} and D_{itf} are the interface trap densities while τ_s and τ_f are the trap time constants for slow and fast traps respectively. In Fig. 4, the trap densities and time constants were extracted from the fitted curves using Eq. (2). As the corresponding peaks for the slow traps occur at much lower than the measurable frequencies, the interface trap density and trap time constant were estimated from the fitting parameters. Similar extraction of parameters has also been reported [21,22]. Typically, fast and slow traps are defined by their time constants, with fast traps having a time constant $<$ 100 μs, while slow traps have a time constant above that. The extracted time constants for fast traps were between 53 and 654 ns, while the slow traps have a time constant of 437 μs to 3 ms. The trap time constants are only used in the extraction of the trap state energies. A similar range of AlN interface state time constants have also been reported elsewhere [8,11]. The trap state energy was estimated using the expression [16]The trap state energy was estimated using equation (3) [20]

$$E_T = -kT\ln(\tau_T \sigma_T v_t N_C) \quad (3)$$

where σ_T is the capture cross-section (3.4×10^{-15} cm^{-2}), ν_t is the thermal velocity of electrons (2.6×10^7 cm s^{-1}), T is the temperature, N_C is the effective density of states at the conduction band in GaN ($4.3 \times 10^{14} \times T^{3/2}$ cm^{-3}), and E_T is the trap state energy below the conduction band [23]. The extracted traps energy levels were located at a depth (E_C-E_T) from 0.24 to 0.56 eV. The estimated D_{it} for both the slow and fast traps are shown in Fig. 5. The fast traps had an estimated D_{it} in the range of 6.7 to 8.2 $\times$ 10^{11} cm^{-2} eV^{-1} within the energy interval of 0.24 to 0.30 eV below the conduction band, while the slow trap D_{it} was in the range of 6.8 to 78.8 $\times$ 10^{11} cm^{-2} eV^{-1} with depth 0.44 to 0.56 eV below the conduction band. The minimum D_{it} (6.7×10^{11} cm^{-2} eV^{-1}) of slow traps is approximately 3.8 $\times$ lower than our previous reported D_{it} (2.6×10^{12} cm^{-2} eV^{-1}) of LTE-AlN/GaN/AlGaN MIS-diode (see Table 1) [15]. This improvement was achieved by optimization of the LTE conditions as mentioned earlier. The fast traps are generally seen in HEMT and are associated with the AlGaN/GaN hetero-interface [11]. The presence of slow traps can be associated with the LTE grown AlN/GaN interface. As the energy of the traps is relative to the Fermi level in the semiconductor, variation of trap energy with voltage can be observed. Variations in time constants with voltage can be used to determine the uniformity of trap states throughout the AlGaN/GaN and AlN/GaN interfaces. If there is an exponential dependence between the two, then there is uniformity in traps throughout the interface. This can be seen as a horizontal line in Fig. 5. Such a horizontal line is present for the fast traps, signifying a uniform distribution of fast traps. However, for the slow traps there is no such exponential dependence. This indicates that the interface states in the AlN layer are not uniformly distributed [23]. A comparison between the minimum D_{it} values obtained in this study and the values using PEALD AlN [11,24] and in-situ MOCVD AlN [8,25] can be seen in Table 1. The measured minimum D_{it} value of LTE-AlN on GaN/AlGaN/GaN is in between the D_{it} values reported using PEALD (3.1×10^{11} to 3×10^{12} cm^{-2} eV^{-1}) as shown in Table 1.

4. Conclusion

In summary, the interface trap characteristics of LTE grown AlN on GaN/AlGaN/GaN MIS-diodes were investigated using the parallel conductance method. The MIS-diode showed two orders of magnitude lower reverse leakage current at -20 V and five orders of magnitude lower forward current at + 2 V as compared to the conventional Schottky diode. The fast traps had an estimated minimum D_{it} of 6.7×10^{11} cm^{-2} eV^{-1} while the slow traps minimum was 6.8×10^{11} cm^{-2} eV^{-1}. The fast traps were located within the energy interval of 0.24 to 0.30 eV below the conduction band while the slow traps were located 0.44 to 0.56 eV below the conduction band. LTE shows D_{it} values in between reported values using PEALD. This study warrants that LTE grown AlN can be used as an alternative method to achieve reasonably low D_{it} values at low temperature which is compatible for mainstream wafer processing.

Data Availability

The raw and processed data required to reproduce these findings are available to download from http://dx.doi.org/10.17632/k6mgyn7hgk.1.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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